AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory device comprising:

a backplane lying upon a substrate;

~~an~~ metal sulfide based media overlying the backplane, the metal sulfide based media comprising an array of selectively conductive memory cells; and

a microactuator assembly operative to move a plurality of probes over the memory cells to facilitate reading, writing, and erasing of selected cells, wherein the reading, writing, and erasing of the memory cell is performed by applying a bias voltage across the memory cell, which causes the memory cell to take on a desired impedance state, the impedance state representing the memory cell.

2. (Original) The memory device of claim 1, further comprising MEMS control circuitry fabricated on the substrate.

3. (Original) The memory device of claim 1, wherein the probes are graphite

4. (Original) The memory device of claim 1, wherein the media is used in conjunction with a polymer.

5. (Original) The memory device of claim 4, wherein the polymer is selected from one of the group consisting of polyacetylene, polyparaphenylene, polythiophene, polypryrrole, and polyaniline, polyphenylacetylene, polydiphenylacetylene.

6. (Original) The memory device of claim 1, wherein the probes are scanning tunneling microscopic probes.

7. (Original) The memory device of claim 6, wherein the probes are operated at a constant distance away from the memory cell.

8. (Original) The memory device of claim 7, wherein the distance between the probe and the memory cell is maintained constant by employing a feedback loop and a microactuated cantilever.

9. (Original) The memory device of claim 1, wherein the probes are in contact the surface of the memory media.

10. (Currently Amended) A memory device comprising:

a metal sulfide based memory media, the memory media comprises a plurality of metal sulfide based memory cells;

an array of probes operative to read, write, and erase the memory media, the reading, writing, and erasing of the memory media is performed by applying a bias voltage across the memory cell, which causes the memory cell to take on a desired impedance state, representing the memory cell; and

controllers for each probe used for formatting the memory media and guiding the motion of the probes.

11. (Original) The memory device of claim 10, wherein the memory media comprises a plurality of metal sulfide based memory cells.

12. (Currently Amended) The memory device of claim 11, wherein each memory cell has a plurality ~~large range~~ of conductivity states at each distinguishable memory cell site.

13. (Original) The memory device of claim 12, wherein each distinguishable memory cell site is determined by size and motion of the probes.

14. (Currently Amended) A memory device comprising:

a substrate;

a planar medium comprising of a metal sulfide based material and a conjugated polymer layer, the planar medium housing a plurality of memory cells;

a backplane lying between the polymer layer and the substrate;

at least one probe facilitating testing the state of the polymer layer; and

a MEMS actuator operative to move the at least one probe over the polymer layer.

15. (Currently Amended) A method for retrieving cell state values, comprising:

positioning microelectromechanical system (MEMS) probes over selected metal sulfide based memory cells;

applying a fixed voltage across a subset of the cells; ~~and~~

determining the impedance of the subset of cells[[.]]; and

programming the metal sulfide memory cells based on the impedance levels.

16. (Original) The method of claim 15, wherein the cell impedance is determined by analyzing tunnel current between the probe and the memory cell.

17. (Original) The method of claim 15, further comprising comparing the measured impedance value with available impedance states to determine the logical state of multiple bits of information contained within the cell.

18. (Currently Amended) A method for programming cell state values, comprising:

positioning microactuated probes over selected metal sulfide based memory cells;

determining a desired impedance state; ~~and~~

applying a threshold voltage across the memory cell corresponding to the desired impedance state[[.]]; and

programming the metal sulfide memory cells based on the impedance states.

19. (Cancelled)

20. (Original) A method of erasing memory cell state values comprising:

positioning probes over selected metal sulfide based memory cells;

measuring the impedance state of the selected memory cells;

determining an impedance state of the memory cells with selected bits erased; and

applying a threshold voltage to the memory cells such that the resulting cell impedance corresponds to the impedance state of the cell with the selective bits erased.

21. (Currently Amended) A memory device comprising:

a metal sulfide based memory media;

means for positioning microactuated probes over selected metal sulfide based memory media to create an array of memory cells;

means for applying bias voltage across the memory cells;

means for determining impedance states of the memory cells;

means for at least one of reading, writing, and erasing the memory media comprising of an array of memory cells; and

means for formatting the memory media.